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STRUCTURE AND METHOD FOR FORMING A FACETED OPENING AND A LAYER FILLING THEREIN

TECHNICAL FIELD

The invention relates generally to semiconductor devices, and more particularly to a structure and method for forming a trench, contact hole, or via, and subsequently depositing a material therein, that is less susceptible to the formation of voids.

BACKGROUND OF THE INVENTION

One type of structure that is commonly found in semiconductor devices is an isolation region, which is used to isolate or prevent current flow between adjacent active regions formed in a semiconductor substrate. Active regions are generally doped regions implanted in a substrate. For example, source/drain regions of a transistor can be considered active regions. An isolation region is formed between the source/drain regions of adjacent transistors to prevent current from flowing from one transistor to the other. This type of isolation region can be found in many conventional memory devices.

One method of forming isolation regions uses a process of the local oxidation of silicon (LOCOS). Typically, a nitride layer is formed on a substrate and subsequently patterned and etched to expose portions of the substrate surface where the isolation regions are to be formed. Thermal oxide is then grown in the exposed areas to form oxide isolation regions. The nitride layer is then removed, and the substrate is ready for device formation in the areas defined by the isolating regions of oxide. This process is well known and will not be described in any greater detail herein. It is enough to note that a shortcoming associated with the LOCOS process is the formation of "bird's beak" spurs that consume lateral area on the surface of a substrate. However, where high density integration of the active regions is desired, sacrificing surface area to accommodate the bird's beak spurs of an isolation region is unacceptable.

An alternative process that does not have the problems associated with LOCOS isolation regions is forming trench-type isolation regions. In this process, rather than performing local oxidation, a trench is formed, and insulating material is deposited therein to form the isolation region. As a result of forming the isolation region by depositing the insulating material into a trench, rather than growing a thermal oxide, the lateral dimensions of the isolation region can be controlled to a much greater degree. Moreover, the formation of bird's beak spurs is no longer an issue since the profile of the trench determines the profile of the isolation region. The conventional process for forming a shallow trench isolation region is generally illustrated by Figure 1.

The process begins with masking and etching a trench 136 through a silicon nitride layer 106, a pad oxide layer 104, and into a substrate 102 (Figures 1a and 1b). As illustrated in Figure 1b, the opening of the trench 136 has a dimension d_1. An layer of insulating material 140 is formed in the trench and over the silicon nitride layer 106 (Figure 1c). An etch process is then performed to etch back the layer of insulating material 140 and the silicon nitride layer 106, leaving the pad oxide layer 104 and an isolation region 142 (Figure 1d). The pad oxide layer 104 is then removed.

As the dimension d_1 is reduced to accommodate the smaller feature sizes of current devices, forming material in the trench 136 becomes more difficult because of step coverage issues. As illustrated in Figure 1c', a void 150 may be formed in the layer of insulating material 140 because of step coverage effects at the opening of the trench 136. As is acknowledged in the art, the creation of voids during the fabrication of semiconductor devices compromise the structure and ultimately the reliability of the devices. Figures 1d' and 1e' illustrate the structure resulting from the conventional process where the void 150 is formed during the formation of the layer of insulating material 140. As previously mentioned, the creation of voids during device fabrication is highly undesirable. Therefore, there is a need for an alternative method for forming an isolation structure that is less susceptible to the formation of voids.

SUMMARY OF THE INVENTION

The present invention is directed to a structure and method for filling an opening in a semiconductor structure that is less susceptible to the formation of voids. A first layer of a first material is formed over the layer in which the opening is to be formed, and a faceted opening is formed in the first layer. The opening in the underlying layer is subsequently formed, and the material that is to fill the opening is deposited over the faceted opening and into the opening of the underlying layer. The faceted opening in the first layer can be formed by performing an isotropic etch on the first layer through an opening in a mask layer that is formed over the first layer.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1a-1e are cross-sectional views of an isolation region at various stages of a conventional process.

Figure 2 is a portion of a process flow diagram for the formation of an isolation region according to an embodiment of the present invention.

Figures 3a-3i are cross-sectional views of an isolation region at various stages according to an embodiment of the present invention.

Figure 4 is a block diagram of a memory device including an isolation region according to an embodiment of the present invention.

As is conventional in the field of integrated circuit representation, the lateral sizes and thicknesses of the various layers are not drawn to scale and may have been enlarged or reduced to improve drawing legibility.

DETAILED DESCRIPTION OF THE INVENTION

Embodiments of the present invention provide a structure and method for forming a trench, contact hole, or via, and subsequently depositing a material therein, that is less susceptible to the formation of voids. Certain details are set forth below to provide a sufficient understanding of the invention. However, it will be clear to one skilled in the art

that the invention may be practiced without these particular details. In other instances, well-known semiconductor fabrication techniques, processing methods, and materials have not been shown in detail in order to avoid unnecessarily obscuring the invention.

An embodiment of the present invention will be described with respect to the process flow illustrated in Figure 2, and the cross-sectional diagrams of Figure 3. The process begins with a structure as illustrated in Figure 3a having a pad oxide layer 304 formed over a substrate 302. As used herein, the term "substrate" or "semiconductor substrate" will be understood to mean any construction comprising semiconductor material, including but not limited to bulk semiconductive materials, such as a semiconductor wafer, and layers of semiconductive material. Further, the term "substrate" also refers to any supporting structure including, but not limited to, the semiconductive substrates described above. As is understood in the art, the pad oxide layer protects the substrate 302 from damage that may occur from subsequent processing steps. The pad oxide layer 304 further promotes adhesion of a subsequently formed silicon nitride layer 306. Formed on the silicon nitride layer 306 is a hard mask layer 310 (Figure 3b). As will be explained in more detail below, the hard mask layer 310 can be formed from a silicon oxide layer using conventional fabrication processes.

The hard mask layer 310 is masked and subsequently etched to form an opening 320 therethrough to expose a portion of the underlying silicon nitride layer 306 (Figure 3c). The photomask used in forming the opening 320 can be the same mask used in the conventional process in forming the trench 136 (Figure 1). Thus, embodiments of the present invention can be implemented without requiring additional masks to be made, and consequently, can be easily integrated into existing process flows.

An isotropic "pull-back" etch is performed on the silicon nitride layer 306 to undercut the silicon nitride layer beneath the opening 320 in the hard mask layer 310. As a result, facets 324 are formed (Figure 3d). The facets 324 are formed because the top portion of the silicon nitride layer 306 near the hard mask layer 310 is etched for the entire time it takes to reach the bottom of the silicon nitride layer 306 near the pad oxide layer

304. It will be appreciated that the material from which the hard mask layer 310 is formed should be relatively resistant to the pull-back etch process. As mentioned previously, a suitable material for the hard mask layer 310 is a silicon oxide material. Moreover, the thickness of the hard mask layer 310 should be selected such that if incidental etching occurs, the remaining thickness of the hard mask layer 310 will be sufficient to provide masking properties during for the pull-back etch process.

The angle of the facets 324 formed from the pull-back etch depend on a variety of factors, such as etch duration, type of etch performed, composition of etchant, and the like. However, as shown in Figure 3d, the angle of the facets 324 are approximately at 45 degrees. Consequently, the thickness of the silicon nitride layer 306 can be used to roughly gauge the increase in the dimension of the opening into which insulating material will be deposited to form the isolation region. As also illustrated in Figure 3d, the pad oxide layer 304 may be partially etched by the pull-back etch.

Following the formation of the facets 324, an etch process is performed to form a trench 330 through the opening 320 in the hard mask layer 310 (Figure 3e). Typically, an anisotropic etch will be performed to form the trench 330. Those of ordinary skill in the art have sufficient understanding to adjust etch parameters to form a trench having the desired dimensions and sidewall profile. The hard mask layer 310 is subsequently removed to fully expose the trench 330 and faceted opening 336 in the silicon nitride layer 306 (Figure 3f). It will be apparent that the dimension d_1' of the faceted opening 336 is greater than the dimension d_1 of the opening 136 (Figure 1) of the conventional process. As a result, deposition of a layer of insulating material 340, such as a silicon oxide material, into the trench 330 to form an isolation region is less likely to result in the formation of a void, which, as previously discussed with respect to the conventional process (Figure 3g), is a concern.

The layer of insulating material 340 and the silicon nitride layer 306 are etched back (Figure 3h) to remove portions of the materials. A conventional chemical-mechanical polishing (CMP) process can be used to etch back the layer of insulating

material 340 and the silicon nitride layer 306. As illustrated in Figure 3h, a portion of the silicon nitride layer 306 remains over the pad oxide layer 304. It will be appreciated that the thickness of any remaining portion of the silicon nitride layer 306 may vary without departing from the scope of the present invention. It will be further appreciated that the etch back of the silicon nitride layer 306 may also continue until the entire layer is removed. Following the etch back process, a conventional etch process can be used to remove any residual silicon nitride. The pad oxide layer 304 is also removed, leaving an isolation region 342 formed in the substrate 302 (Figure 3i).

As illustrated in Figure 3i, the dimensions d_2' and d_3' of the isolation region 342 may be substantially equal to the dimensions d_2 and d_3, respectively, of the isolation region 142 (Figure 1) formed through the conventional process previously discussed. Thus, although embodiments of the present invention provide a structure and process less susceptible to the formation of voids when forming material within a trench, the dimension of any active regions adjacent to the isolation region can still be maintained.

As previously mentioned, embodiments of the present invention provide the advantage of being easily integrated into current process flows because existing photomasks can be used. Moreover, because the facets 324 are formed through an isotropic etch process, no additional masking steps need to be added to existing processes.

It will be appreciated that additional process steps can be included in embodiments of the present invention without departing from the scope of the present invention. For example, with respect to the previous example of forming a trench-type isolation region, implant steps may be performed following the formation of the trench 330 and prior to the formation of the layer of insulating material 340 to provide further channel stop capabilities.

Although the previous embodiment of the present invention was directed to the formation of an isolation region, it will be appreciated that some or all of the principles of the present invention can be used generally for the formation of a trench and the subsequent deposition of material therein. For example, embodiments of the present

invention can be applied in the formation of a trench capacitor, or alternatively, in the formation of conductive interconnects. It will be further appreciated that embodiments of the present invention can also be used in the formation of contact holes or vias, and the subsequent deposition of a conductive material therein. Generally, some or all of the principles of the present invention can be applied where the dimensions of an opening are such that step coverage of a material deposited into the opening may result in the formation of voids.

A memory device 400 that includes isolation regions according to an embodiment of the invention is shown in Figure 4. The isolation regions are present in a memory array 402. The memory device 400 includes a command decoder 406 that receives memory command through a command bus 408 and generates corresponding control signals. A row or column address is applied to the memory device 400 through an address bus 420 and is decoded by a row address decoder 424 or a column address decoder 428, respectively. Memory array read/write circuitry 430 are coupled to the array 402 to provide read data to a data output buffer 434 via a input-output data bus 440. Write data are applied to the memory array through a data input buffer 444 and the memory array read/write circuitry 430.

From the foregoing it will be appreciated that, although specific embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention. Accordingly, the invention is not limited except as by the appended claims.